CUSCLIB Cell list – Jan 2020

* The Status column indicates an error that should be corrected. Other comments indicates how this cell can be improved.
* Note the logic expression of each cell in library layout file (CUSCLIB full Jan 2020.tdb)­
* There should be no entities outside cell boundaries (e.g., rulers)
* Problem cells are mostly due to absence of plugs .
* D FF and T FF are implemented in three different sizing­­
  1. W/L n = 1, W/L p = 3
  2. W/L n = 1, W/L p = 2
  3. W/L n = 1, W/L p = 1.5
* The Status “OK” means the cell is functionally correct. It does not mean that the cell layout or performance is “Good” !

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| index | Gate | description | W/L for  NMOS Tr. | W/L for PMOS Tr. | Status |
| 1 | Inverter, Buffer | Two different cells: an inveter and a buffer | 1/1 | 1/1 | OK |
| 2 | Inverter, Buffer | Two different cells: an inveter and a buffer | 1/1 | 2/1 | OK |
| 3 | Inverter, Buffer | Two different cells: an inveter and a buffer | 1/1 | 3/1 | OK |
| 4 | Inverter, Buffer | Two different cells: an inveter and a buffer | 1/1 | 4/1 | OK |
| 5 | NAND | 2 input Nand Gate | 1/1 | 1/1 | OK. |
| 6 | NAND | 2 input Nand Gate | 1/1 | 2/1 | OK |
| 7 | NAND | 2 input Nand Gate | 1/1 | 3/1 | OK |
| 8 | NAND | 2 input Nand Gate | 1/1 | 4/1 | OK |
| 9 | NAND | 3 input Nand Gate | 1/1 | 1/1 | OK |
| 10 | NAND | 3 input Nand Gate | 1/1 | 2/1 | OK |
| 11 | NAND | 3 input Nand Gate | 1/1 | 3/1 | OK |
| 12 | NAND | 3 input Nand Gate | 1/1 | 4/1 | OK |
| 13 | NAND | 4 input Nand Gate | 1/1 | 1/1 | OK |
| 14 | NAND | 4 input Nand Gate | 1/1 | 2/1 | OK |
| 15 | NAND | 4 input Nand Gate | 1/1 | 3/1 | OK |
| 16 | NAND | 4 input Nand Gate | 1/1 | 4/1 | OK |
| 17 | NOR | 2 input NOR Gate | 1/1 | 1/1 | OK |
| 18 | NOR | 2 input NOR Gate | 1/1 | 2/1 | OK |
| 19 | NOR | 2 input NOR Gate | 1/1 | 3/1 | OK |
| 20 | NOR | 2 input NOR Gate | 1/2 | 1/1 | OK. |
| 21 | NOR | 3 input NOR Gate | 1/1 | 1/1 | OK |
| 22 | NOR | 3 input NOR Gate | 1/1 | 2/1 | OK |
| 23 | NOR | 3 input NOR Gate | 1/1 | 3/1 | OK |
| 24 | NOR | 3 input NOR Gate | 1/2 | 1/1 | Ok |
| 25 | NOR | 4 input NOR Gate | 1/1 | 1/1 | OK |
| 26 | NOR | 4 input NOR Gate | 1/1 | 2/1 | OK |
| 27 | NOR | 4 input NOR Gate | 1/1 | 3/1 | OK |
| 28 | NOR | 4 input NOR Gate | 1/2 | 1/1 | OK |
| 29 | Xor | 2 input Xor Gate | 1/1 | 1/1 | OK |
| 30 | Xor | 2 input Xor Gate | 1/1 | 2/1 | OK |
| 31 | Xor | 2 input Xor Gate | 1/1 | 3/1 | OK |
| 32 | Xor | 2 input Xor Gate | 1/2 | 1/1 | OK |
| 33 | Xnor | 2 input Xnor Gate | 1/1 | 1/1 | OK |
| 34 | Xnor | 2 input Xnor Gate | 1/1 | 2/1 | OK |
| 35 | Xnor | 2 input Xnor Gate | 1/1 | 3/1 | OK |
| 36 | Xnor | 2 input Xnor Gate | 1/2 | 1/1 | OK |
| 37 | Dynamic SR | Inverter wiht Pass transistor | 1/1 | 1/1 | OK. |
| 38 | Dynamic SR | Inverter wiht Pass transistor | 1/1 | 2/1 | OK |
| 39 | Dynamic SR | Inverter wiht Pass transistor | 1/1 | 3/1 | OK |
| 40 | Dynamic SR | Inverter wiht Pass transistor | 1/2 | 1/1 | OK |
| 41 | Dynamic SR | Inverter with TG | 1/1 | 1/1 | OK |
| 42 | Dynamic SR | Inverter with TG | 1/1 | 2/1 | OK |
| 43 | Dynamic SR | Inverter with TG | 1/1 | 3/1 | OK |
| 44 | Dynamic SR | Inverter with TG | 1/2 | 1/1 | OK |
| 45 | AND-OR-INVERT | 2x2-Input AND into 2-Input NOR | 1/1 | 1/1 | OK |
| 46 | AND-OR-INVERT | 2x2-Input AND into 2-Input NOR | 1/1 | 2/1 | OK |
| 47 | AND-OR-INVERT | 2x2-Input AND into 2-Input NOR | 1/1 | 3/1 | OK |
| 48 | AND-OR-INVERT | 2x2-Input AND into 2-Input NOR | 1/2 | 1/1 | OK. |
| 49 | AND-OR-INVERT | 2-Input AND into 2-Input NOR | 1/1 | 1/1 | OK |
| 50 | AND-OR-INVERT | 2-Input AND into 2-Input NOR | 1/1 | 2/1 | OK |
| 51 | AND-OR-INVERT | 2-Input AND into 2-Input NOR | 1/1 | 3/1 | OK |
| 52 | AND-OR-INVERT | 2-Input AND into 2-Input NOR | 1/2 | 1/1 | OK |
| 53 | AND-OR-INVERT | 2-Input AND into 3-Input NOR | 1/1 | 1/1 | OK |
| 54 | AND-OR-INVERT | 2-Input AND into 3-Input NOR | 1/1 | 2/1 | OK |
| 55 | AND-OR-INVERT | 2-Input AND into 3-Input NOR | 1/1 | 3/1 | OK |
| 56 | AND-OR-INVERT | 2-Input AND into 3-Input NOR | 1/2 | 1/1 | OK |
| 57 | AND-OR-INVERT | 3-Input AND into 2-Input NOR | 1/1 | 1/1 | OK |
| 58 | AND-OR-INVERT | 3-Input AND into 2-Input NOR | 1/1 | 2/1 | OK |
| 59 | AND-OR-INVERT | 3-Input AND into 2-Input NOR | 1/1 | 3/1 | poor layout |
| 60 | AND-OR-INVERT | 3-Input AND into 2-Input NOR | 1/2 | 1/1 | OK |
| 61 | Majority | Majority (AB+AC+BC) | 1/1 | 1/1 | OK |
| 62 | Majority | Majority (AB+AC+BC) | 1/1 | 2/1 | OK |
| 63 | Majority | Majority (AB+AC+BC) | 1/1 | 3/1 | OK |
| 64 | Majority | Majority (AB+AC+BC) | 1/2 | 1/1 | OK |
| 65 | Inverting Majority | ~(AB+AC+BC) | 1/1 | 1/1 | OK |
| 66 | Inverting Majority | ~(AB+AC+BC) | 1/1 | 2/1 | Ok |
| 67 | Inverting Majority | ~(AB+AC+BC) | 1/1 | 3/1 | OK |
| 68 | Inverting Majority | ~(AB+AC+BC) | 1/2 | 1/1 | OK |
| 69 | OR-AND-INVERT | 2- Input OR into 2-Input NAND | 1/1 | 1/1 | OK |
| 70 | OR-AND-INVERT | 2- Input OR into 2-Input NAND | 1/1 | 2/1 | OK |
| 71 | OR-AND-INVERT | 2- Input OR into 2-Input NAND | 1/1 | 3/1 | OK |
| 72 | OR-AND-INVERT | 2- Input OR into 2-Input NAND | 1/2 | 1/1 | OK |
| 73 | OR-AND-INVERT | 2- Input OR into 3-Input NAND | 1/1 | 1/1 | OK |
| 74 | OR-AND-INVERT | 2- Input OR into 3-Input NAND | 1/1 | 2/1 | OK |
| 75 | OR-AND-INVERT | 2- Input OR into 3-Input NAND | 1/1 | 3/1 | OK |
| 76 | OR-AND-INVERT | 2- Input OR into 3-Input NAND | 1/2 | 1/1 | OK |
| 77 | OR-AND-INVERT | 2x2-Input OR into 2-Input NAND | 1/1 | 1/1 | OK |
| 78 | OR-AND-INVERT | 2x2-Input OR into 2-Input NAND | 1/1 | 2/1 | OK |
| 79 | OR-AND-INVERT | 2x2-Input OR into 2-Input NAND | 1/1 | 3/1 | OK |
| 80 | OR-AND-INVERT | 2x2-Input OR into 2-Input NAND | 1/2 | 1/1 | OK |
| 81 | OR-AND-INVERT | 3-Input OR into 2-Input NAND | 1/1 | 1/1 | OK |
| 82 | OR-AND-INVERT | 3-Input OR into 2-Input NAND | 1/1 | 2/1 | OK |
| 83 | OR-AND-INVERT | 3-Input OR into 2-Input NAND | 1/1 | 3/1 | OK |
| 84 | OR-AND-INVERT | 3-Input OR into 2-Input NAND | 1/2 | 1/1 | OK |
| 85 | Multiplexer | 2:1 multiplexer | 1/1 | 1/1 | OK |
| 86 | Multiplexer | 2:1 multiplexer | 1/1 | 2/1 | OK |
| 87 | Multiplexer | 2:1 multiplexer | 1/1 | 3/1 | OK |
| 88 | Multiplexer | 2:1 multiplexer | 1/2 | 1/1 | OK |
| 89 | Inverting Multiplexer | Inverting 2:1 Multiplexer | 1/1 | 1/1 | OK |
| 90 | Inverting Multiplexer | Inverting 2:1 Multiplexer | 1/1 | 2/1 | OK |
| 91 | Inverting Multiplexer | Inverting 2:1 Multiplexer | 1/1 | 3/1 | OK |
| 92 | Inverting Multiplexer | Inverting 2:1 Multiplexer | 1/2 | 1/1 | OK |
| 93 | 1 bit Comparator cell | Equality output | 1/1 | 1/1 | OK |
| 94 | 1 bit Comparator cell | Equality output | 1/1 | 2/1 | OK |
| 95 | 1 bit Comparator cell | Equality output | 1/1 | 3/1 | OK |
| 96 | 1 bit Comparator cell | Equality output | 1/2 | 1/1 | OK |
| 97 | ADDER | Half adder | 1/1 | 1/1 | OK |
| 98 | ADDER | Half adder | 1/1 | 2/1 | Poor logic implementation, |
| 99 | ADDER | Half adder | 1/1 | 3/1 | OK |
| 100 | ADDER | Half adder | 1/2 | 1/1 | Poor logic implementation |
| 101 | D-FF | Slave cell of static D FF |  |  | OK |
| 102 | D-FF | Master cell of static D FF |  |  | OK |
| 103 | T-FF | Slave cell of static T FF |  |  | OK |
| 104 | T-FF | Master cell of static T FF |  |  | OK |